23mΩ OVP Switch with OTG Function

General Description

The ET9902 is a high voltage, high current, bidirectional switch. It provides input over-voltage and surge protection as well as reverse-blocking of output voltage. The logic control of the device is designed to interact with both the system controller and the wireless charging receiver which allows creating a dual input charger application with a single switch.

The device is packaged in advanced WLCSP20, which is ideal for small form factor portable equipment .

Features

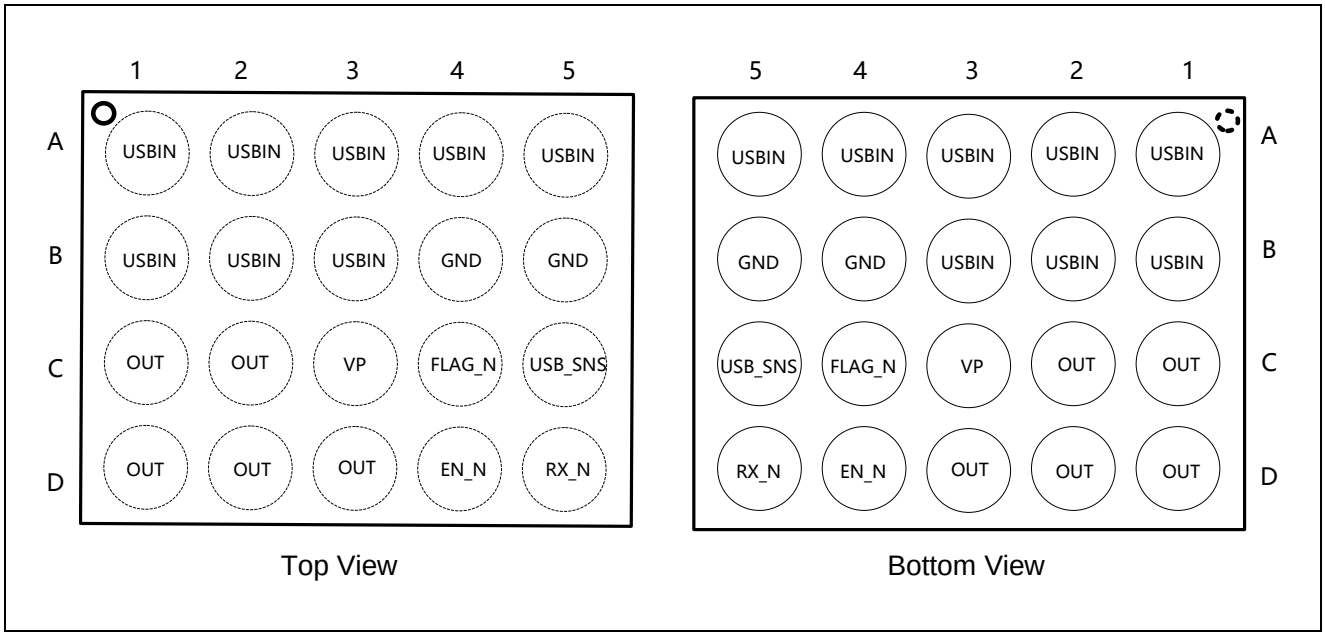
- Operating range from 3.6V to 20V
- Absolute maximum voltage of V_{IN} up to 28V
- Pin-selectable over-voltage protection(13V/17V)
- Input voltage sense output with selectable clamp(16V/20V)
- Low RDS(on) is 23mΩ typical at V_{IN}=5V/1A
- 5A DC Nominal and 7A maximum current capability
- Autonomous mode and slave mode operation
- 50ms Input supply detect deglitcher in autonomous mode
- 50ms Break-before-make timing with discharge
- Bi-directional status indicator and OTG enable pin
- Device enable input (active low)
- Wireless enable output (active low)
- Surge immunity to ±100V
- Compliance to IEC61000−4−2 (Level 4): bypassed with a 1.0μF or larger capacitor
  -- 15kV Pass (Air) , 8kV Pass (Contact), ESD Ratings: HBM >2.5kV
- Pat No. and Package

Part No.	Package
ET9902	WLCSP20 (1.67mm × 2.24mm, ball pitch=0.4mm)

Applications

- Smartphones, Tablet PC
- HDD, Storage, and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

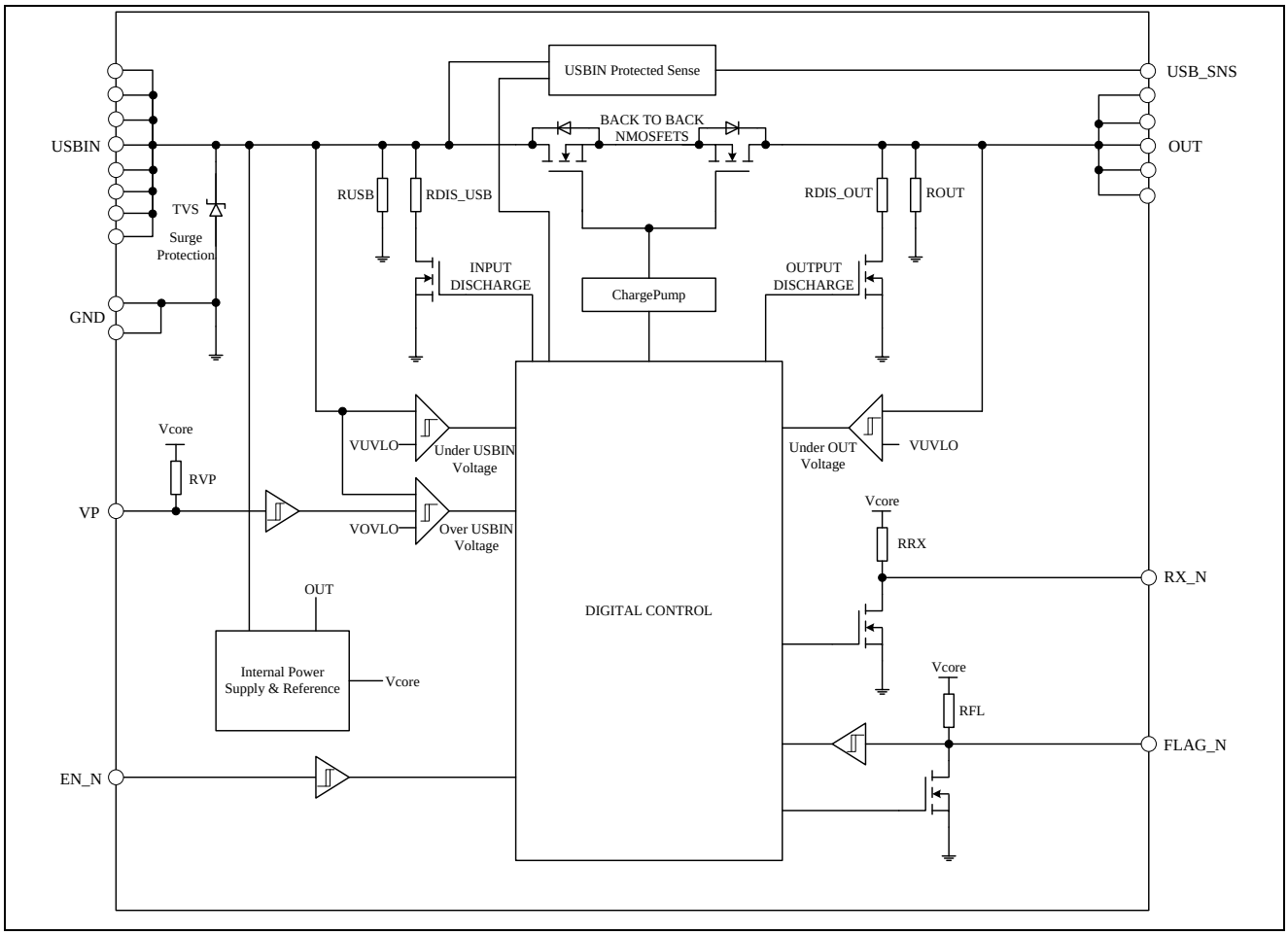
Pin Configuration



Pin Function

Pin No.	Pin Name	Function
A1~A5, B1~B3	USBIN	Load Switch Input
C1,C2, D1~D3	OUT	Load Switch Output
C5	USB_SNS	Clamped USBIN Sense Output
C3	VP	Over-voltage Protection Setting
D4	EN_N	Active Low Logic Enable
D5	RX_N	Wireless Receiver Active Low Enable
C4	FLAG_N	OTG Enable Input/Ready for OTG Output
B4, B5	GND	Ground

Block Diagram



Functional Description

Traditionally mobile phones and other portable equipment can get charged from a single power source such as USB. With the growing popularity of wireless charging, consumers like to be able to charge from both USB and a wireless source. Most mobile phone chipsets are not capable to natively charge from these two sources. In order to accommodate those chipsets, an input selector switch or multiplexer can be added such as the ET9902. However, in combination with some wireless charger receivers a single switch could suffice. This is the case if the wireless receiver can be disabled and if it provides reverse blocking of the voltage coming from USB. The ET9902 perfectly fits to this application.

Voltage Protection

The voltage protection includes surge protection, over-voltage protection, and voltage protected sense output.

The surge protection at USBIN protects the application against surges that may occur on the USB input. The protection level is in compliance with the IEC 61000-4-5 1.2/50us and 5/20us surge waveforms up to 100V. The ground balls GND should be solidly routed to the ground plane to guarantee robustness.

To protect the system against to high DC or transient voltages, the switch of the ET9902 is opened when an over-voltage is detected. The switch is opened a-synchronously to and has no direct influence on the state

machine. The over-voltage detection level is select-able by means of the VP pin. With VP to ground, the highest over-voltage protection level is selected. With VP left floating the lowest setting is selected.

The voltage at the USB port is to be sensed by the system. However, for the very same reasons as listed above, the voltage at the sense pin of the system will have to be limited. For this purpose, USB_SNS provides a voltage protected version of USBIN. USB_SNS pin accurately tracks the voltage at USBIN but is clamped to a maximum level that is selected with the VP pin.

Operating Modes

System wise the ET9902 can operate autonomously or be used as a slave.

In autonomous mode the switch is opened and closed based on the presence of USBIN. For autonomous mode the EN_N pin is to be connected to ground or forced low by other means. The RX_N pin is connected to the wireless receiver and FLAG_N connected to the system.

A break before make mechanism will ensure proper initialization of the system. If no USBIN is present, the RX_N pin will be low and the wireless receiver enabled. Upon USBIN detection the wireless receiver is disabled by making RX_N high by pulling this pin up to the core voltage through an on-chip resistor. After having actively discharged OUT, the switch will be closed. When the voltage at USBIN is removed the device will power down and the wireless receiver will automatically be re-enabled.

For OTG operation the bi-directional FLAG_N pin is used. Under normal situations, the FLAG_N pin is actively pulled low by the device. When the system applies a valid voltage to OUT, the device will verify if no USB voltage is present in absence of a valid USB voltage, FLAG_N will be released and pulled up through an on-chip resistor to the core voltage. The system can now close the switch by forcing FLAG_N low which will provide the voltage at OUT to USBIN. The USB peripheral connected will get supplied while at the same time the device makes the RX_N pin high, disabling the wireless receiver. The system can re-open the switch by releasing the FLAG_N which will also make the RX_N pin low again.

In slave mode the switch is opened and closed by controlling the EN_N pin. The RX_N and FLAG_N pins are not connected to the system and can be connected to grounds or be left floating. The state of both RX_N and FLAG_N will follow the same scheme as applied for the autonomous mode. For slave mode to be detected the EN_N pin is to be high at the instant USBIN or OUT is applied or should be made high shortly after, see also the flow diagram below.

The wireless receiver can provide a regulated 5V to OUT, not only for supplying the system but also to support OTG operation. This is referred to as concurrent OTG mode. If the autonomous mode was used for this it would automatically disable the wireless receiver through RX_N as described above. Therefore, if concurrent OTG mode is desired, the slave mode operation is to be used. In slave mode, the FLAG_N pin can be monitored by the system so that based on this information it can decide when make EN_N low and thus close the switch.

Flow Diagram

Below flow diagram reflects the operation of the state machine of the ET9902. In combination with the label definitions as listed in the table afterwards, it provides more details on the above described behavior.

The state machine can only operate if the core of the ET9902 is sufficiently supplied from either USBIN or

OUT. In both cases, the voltage will have to be above the undervoltage threshold. In case the core is not or no longer supplied, the state machine is in the OFF state. This may typically occur upon removal of a supplied USB cable.

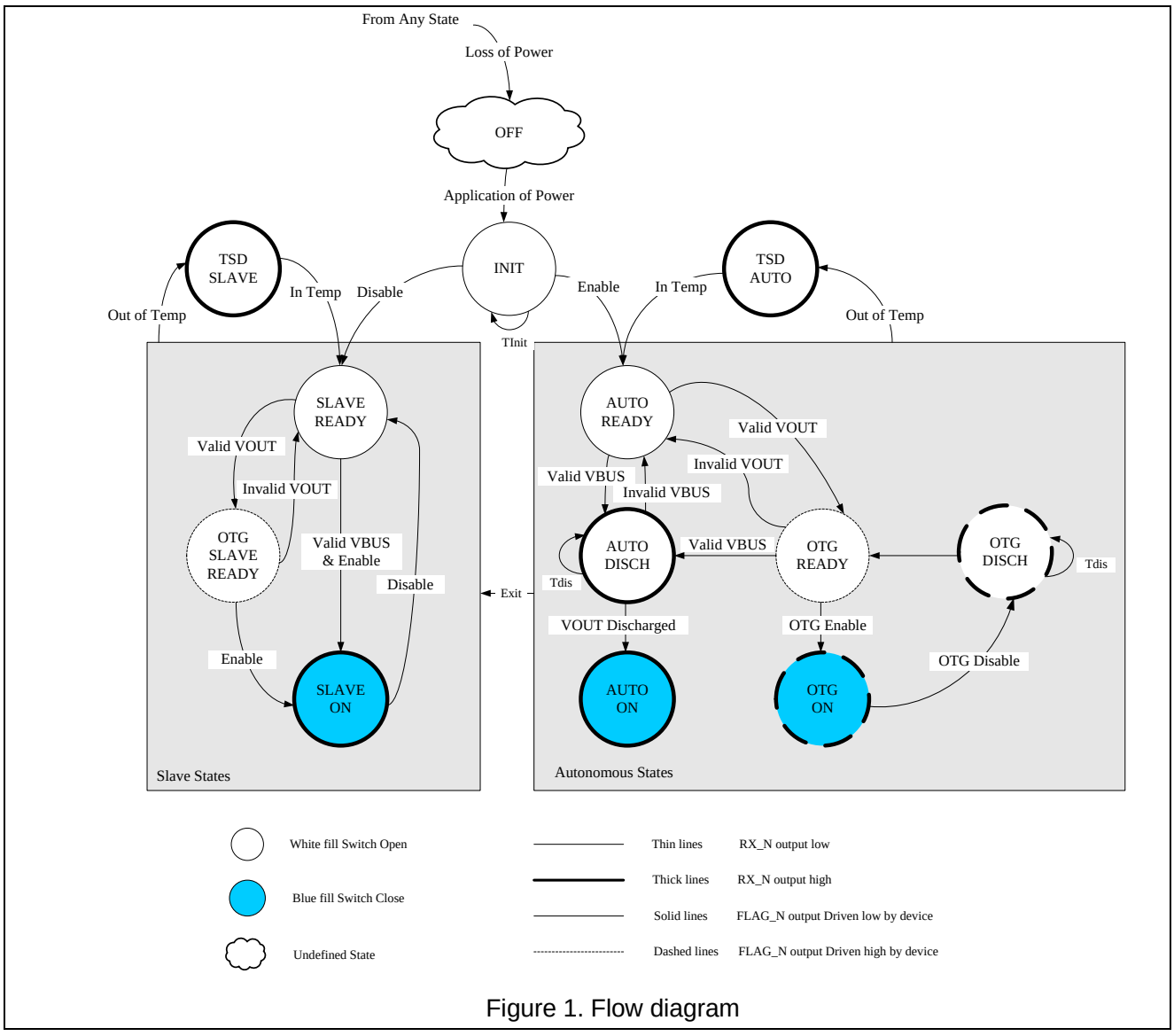


Figure 1. Flow diagram

Acronyms and Definitions

Label	Description
Loss of power	Both USBIN and OUT below the UVLO threshold
Application of Power	USBIN and/or OUT above the UVLO threshold
Enable	EN_N pin is low, debounced for Tilen
Disable	EN_N pin is high, debounced for Tihen
Valid VBUS	USBIN above the UVLO threshold debounced for Tdebusb, the OUT voltage don't care
Invalid VBUS	Inverted signal of 'Valid VBUS'
Valid VOUT	OUT above the UVLO threshold debounced for Tdebout and no 'Valid VBUS'
Invalid VOUT	Inverted signal of 'Valid VOUT'
VOUT Discharged	OUT below the UVLO threshold, no debounce
OTG Enable	FLAG_N pin is forced low by the system while FLAG_N was pulled high by the device, debounced for Tilfl
OTG Disable	FLAG_N pin is released by system and FLAG_Nis pulled up by the device, debounced for Tihfl
Out of Temp	Die temperature exceeds thermal shutdown threshold
In Temp	Die temperature falls below thermal shutdown threshold
Tinit	Power up and initialization duration
Tdis	Discharge duration
OFF	Device is not powered
INIT	EN_N don't care, Switch open, RX_N and FLAG_N low. Startup of the device including analog and digital blocks an reading of OTP fused. Duration Tinit.
TSD SLAVE	EN_N don't care, Switch open, RX_N high, FLAG_N low Entered from any slave state at Out of Temp conditions
TSD AUTO	EN_N low, Switch open, RX_N high, FLAG_N low Entered from any autonomous state at Out of Temp conditions
AUTO READY	EN_N low, Switch open, RX_N and FLAG_N low Autonomous mode is detected during INIT state. Can also be entered from AUTO DISCH(if invalid VBUS)
AUTO DISCH	EN_N low, Switch open, RX_N high, FLAG_N low A 'Valid VBUS' is detected, discharge load activated on OUT and USBIN, minimum duration Tdis. The 'VOUT Discharged' condition must be met before exiting for AUTO ON (verification done for safety reasons)
AUTO ON	EN_N low, Switch closed, RX_N high, FLAG_N low Under normal conditions this state is only exited upon loss of power (eg. USB removal)
OTG READY	EN_N low, Switch open, RX_N low, FLAG_N high A 'Valid VOUT' is detected
OTG ON	EN_N low, Switch closed, RX_N high, FLAG_N forced low by the system An 'OTG enable' condition is detected

OTG DISCH	EN_N low, Switch open, RX_N high, FLAG_N high (no longer forced low by the system)Discharge load activated on OUT and USBIN, duration Tdis, exited for OTG READY
SLAVE READY	EN_N high, Switch open, RX_N and FLAG_N low Slave mode is detected during INIT state. Can also be entered from certain autonomous states if EN_N was initially low upon exiting the INIT state
OTG SLAVE READY	EN_N high, Switch open, RX_N low, FLAG_N high , A 'Valid VOUT' is detected
SLAVE ON	EN_N low, Switch closed, RX_N high, FLAG_N low
Exit	While in one of the autonomous states, EN_N is made high leading to an Exit to a slave state. The mapping of the states is as follows: AUTO READY, AUTO DISCH → SLAVE READY AUTO ON, OTG ON, OTG DISCH → SLAVE READY OTG READY → OTG SLAVE READY
***Note*:** Over-voltage detection does not have a direct influence on the state machine, it will only open the switch	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min	Max	Unit
V_{USBIN}	USBIN to GND			-0.3	28	V
V_{USB_SNS}	USB_SNS to GND			-0.3	20	V
V_{OUT}	OUT to GND			-0.3	20	V
V_{CTRL}	VP, EN_N, RX_N, FLAG_N to GND			-0.3	6	V
I_{SW1}	Maximum Continuous Current of Switch USBIN-OUT				5	A
I_{SW2}	Maximum Peak Current of Switch USBIN-OUT(10ms)				10	A
T_{STG}	Storage Temperature			-65	+150	°C
ESD	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	15.0		KV
			Contact Discharge	8.0		
		Human Body, ANSI/ESDA/JEDEC JS-001-2012	All Pins	>2.5		
		Charged Device Model, JESD22-C101	All Pins	>1.0		
Surge		IEC 61000-4-5, Surge Protection	USBIN	-100	100	V

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Unit
V_{USBIN}	Operational Power Supply on USBIN	0		28	V
V_{VP} V_{EN} V_{RX} V_{FLAG}	VP, EN_N, RX_N, FLAG_N Operational Supply	0		5.5	V
I_{OUT}	Operational Output Current	0		5	A
V_{OUT}	Operational Supply on OUT (OTG mode, USBIN=0V)	0		5.5	V
C_{USBIN}			1		uF
C_{USB_SNS}			1		uF
C_{OUT}		0.1			uF
$R_{\theta JA}$	(1) (2)		55		°C/W
T_J		-40	25	+125	°C
T_A	Operating Temperature Range	-40		+85	°C

Notes：

1. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.

2. The $R_{\theta JA}$ is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p 57mm×51mm 1oz JEDEC PCB standard.

Electrical Characteristics

Unless otherwise noted, min & max limits apply for a T_A between 40°C and +85°C, T_J up to +125°C.Typical values are referenced to T_A = +25°C. Supply conditions V_{USBIN} = 5V, V_{OUT} = 5V. Capacitor values (DC Bias 0 V) C_{USBIN} = 1uF, C_{OUT} = 1uF, C_{USB_SNS} = 1uF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TVS Characteristics						
V_{BR}	Reverse Breakdown Voltage	I_T=10mA, T_A=25°C	29	32	36	V
I_{PP}	Peak Pulse Current(5)	t_p=8/20μs(+100V), T_A=25°C	28	32.5	36	A
V_C	Clamping Voltage(5)	I_{PP}=32.5A, t_p=8/20μs, T_A=25°C	31	35	40	V
I_{PP_NEG}	Reverse Peak Pulse Current(5)	t_p=8/20μs(-100V surge) , T_A=25°C	-55	-48.5	-40	A
V_{C_NEG}	Reverse Clamping Voltage(5)	I_{PP}=-49A, t_p=8/20μs, T_A=25°C	-5	-2	-1	V
V_F	Forward Voltage	I_F=10mA, T_A=25°C	0.2	0.6	0.9	V
Basic Operation						
V_{UVLO_USB}	Under Voltage Lockout at USBIN	Rising, T_A=25°C	2.55	2.8	3.3	V
		Falling, T_A=25°C	2.45	2.6	3.1	V
$V_{UVLOHYS\_USB}$	UVLO hysteresis of USBIN			0.3		V
V_{UVLO_OUT}	Under Voltage Lockout at OUT	Rising, T_A=25°C	2.55	2.8	3.3	V
		Falling, T_A=25°C	2.45	2.6	3.1	V

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{UVLOHYS\_OUT}$	UVLO hysteresis of OUT			0.3		
V_{CORE}	Core Voltage	On chip core voltage	2.45	3.4	4.5	V
V_{OVP}	Over Voltage Lockout at USBIN	Rising, VP to ground (3)	16	17	18	V
		Rising, VP left floating (3)	12	13	14	V
V_{OVP_HYS}	Over Voltage Lockout Hysteresis			300		mV
R_{DSON}	Switch On Resistance	From USBIN to OUT, T_A=25°C		23	35	mΩ
R_{USB}	Termination Resistance at USBIN	Always connected	120	220	320	kΩ
R_{DIS_USB}	Discharge Resistance at USBIN	During discharge states		500		Ω
V_{LK_USBIN}	Switch Input to Output Leakage	Switch not conducting, V_{USBIN} = 28V, OUT not loaded			0.4	V
R_{OUT}	Termination Resistance at OUT	Always connected	120	220	320	kΩ
V_{LK_OUT}	Switch Output to Input Leakage	Switch not conducting, V_{OUT} = 16V, USBIN not loaded			0.4	V
R_{DIS_OUT}	Discharge Resistance at OUT	During discharge states		500		Ω
$V_{SNSCLMP}$	Voltage Clamp at USB_SNS	Rising, VP to ground (3)	16		20	V
		Rising, VP left floating (3)	12		16	V
dV_{SNS}	Voltage Drop at USB_SNS	Referenced to USBIN, Load 20mA		20	37	mV
I_{Q_USBIN}	Input Quiescent Current	Switch not conducting, V_{USBIN}=5V		110	200	uA
I_{DD_USBIN}	Input Operating Current	Switch conducting, V_{USBIN} = 5V		140	250	uA
I_{Q_OUT}	Output Quiescent Current	Switch not conducting, V_{OUT} = 5V		110	200	uA
I_{DD_OUT}	Output Operating Current	Switch conducting, V_{OUT} = 5V		140	250	uA
V_{IH}	Input Logic High Level	EN_N, FLAG_N, VP	1.4		5.5	V
V_{IL}	Input Logic Low Level	EN_N, FLAG_N, VP	0		0.4	V
I_{LK_EN}	Input Leakage Current EN_N	V_{EN_N}=5V, V_{USBIN} =0V, V_{OUT} =0V			1	uA
		V_{EN_N} =5V, V_{USBIN} =5V, V_{OUT} =0V			1	uA
V_{OL}	Output Logic Low Level	FLAG_N, RX_N, Sink 2mA			0.2	V
R_{FL}	Logic High Pull Up FLAG_N	FLAG_N to VCORE	350	500	750	kΩ

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{RX}	Logic High Pull Up RX_N	RX_N to VCORE	350	500	750	kΩ
R_{VP}	Logic High Pull Up VP	VP to VCORE	350	500	750	kΩ
T_{IHEN}	Input Logic High Debounce	EN_N		40		us
T_{ILEN}	Input Logic Low Debounce	EN_N		40		us
T_{IHFL}	Input Logic High Debounce	FLAG_N		40		us
T_{ILFL}	Input Logic Low Debounce	FLAG_N		40		us
T_{DEBUSB}	Supply Debounce Period	Debounce of USBIN		50		ms
T_{DEBOUT}	Supply Debounce Period	Debounce of OUT(5)		40		us
T_{DIS}	Supply Discharge Period	Discharge of USBIN and OUT		50		ms
dT	Timing Accuracy	(4)	20		+20	%
T_{INIT}	Power Up and Initialization Period	Upon USBIN or OUT crossing UVLO		150		us
T_{SNS}	Startup Time USB_SNS	V_{USBIN} = 5V, USB_SNS from 0V to 4.5V, not loaded			500	us
T_{SSTART}	Switch Soft Start Timing	V_{USBIN} = 5V, OUT from 10 % to 90 % of USBIN		1	3	ms
		V_{OUT} = 5V, USBIN from 10 % to 90 % of OUT		1	3	ms
T_{UVLO}	Input Falling Disable Delay	Delay from UVLO falling edge to disabling the load switch		10	20	us
T_{OVP}	Input Rising Disable Delay	Delay from OVLO rising edge to disabling the load switch (5)		100		ns
T_{SD}	Thermal Shutdown	Rising (5)		150		°C
		Falling (5)		115		

Notes:

3. Includes DC operation as well as USBIN from 0 V to 28 V in 3 V/us, USBIN from 5 V to 28 V in 1.5 V/us and 100 V surge hold off (IEC61000-4-5) 1.2/50us and 5/20us.

4. Timing accuracy valid for T_{IHEN}, T_{ILEN}, T_{IHFL}, T_{ILFL}, T_{DEBUSB}, T_{DEBOUT}, T_{DIS} through internal clock measurement.

5. This parameter is guaranteed by design and characterization.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Timing Diagrams

The below timing diagrams reflect the behavior of the state machine described above. They are intended for illustration purposes only.

Note: timings are not on scale.

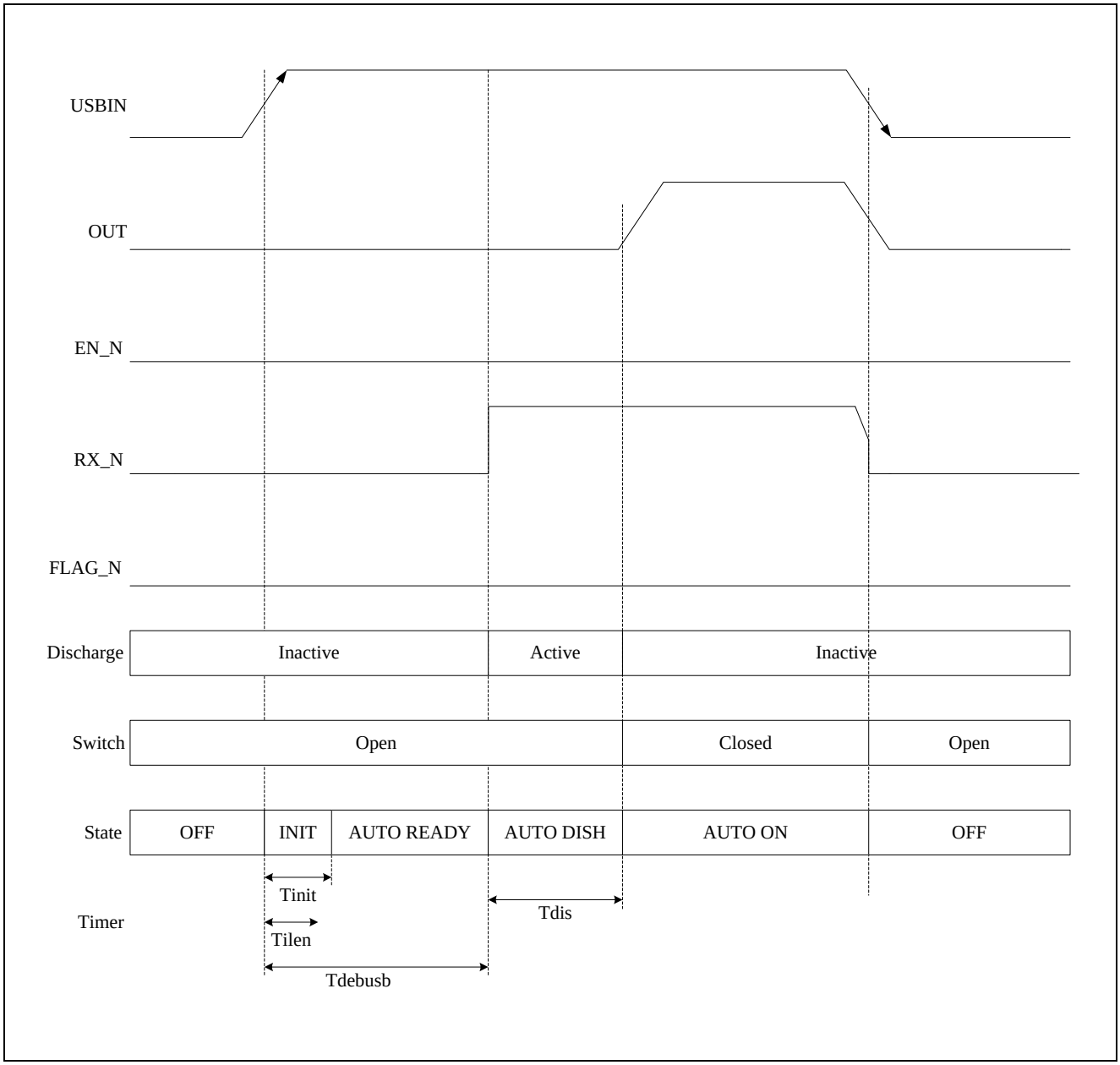


Figure 2. Autonomous configuration. Application of VBUS with system turned off, removal of VBUS

Timing Diagrams(Continued)

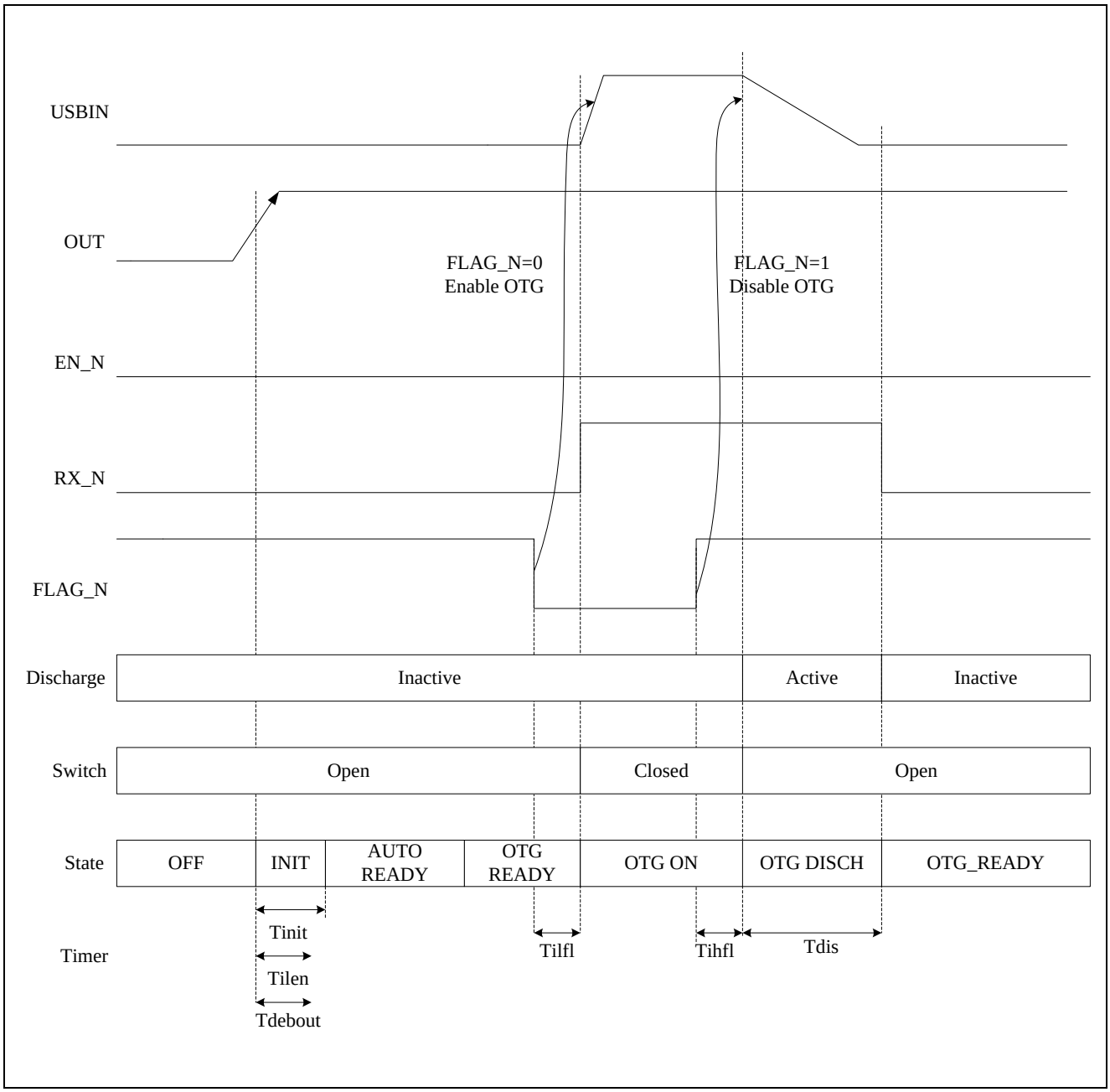


Figure 3. Autonomous configuration. Application of VOUT, enabling(OTG), disabling

Timing Diagrams(Continued)

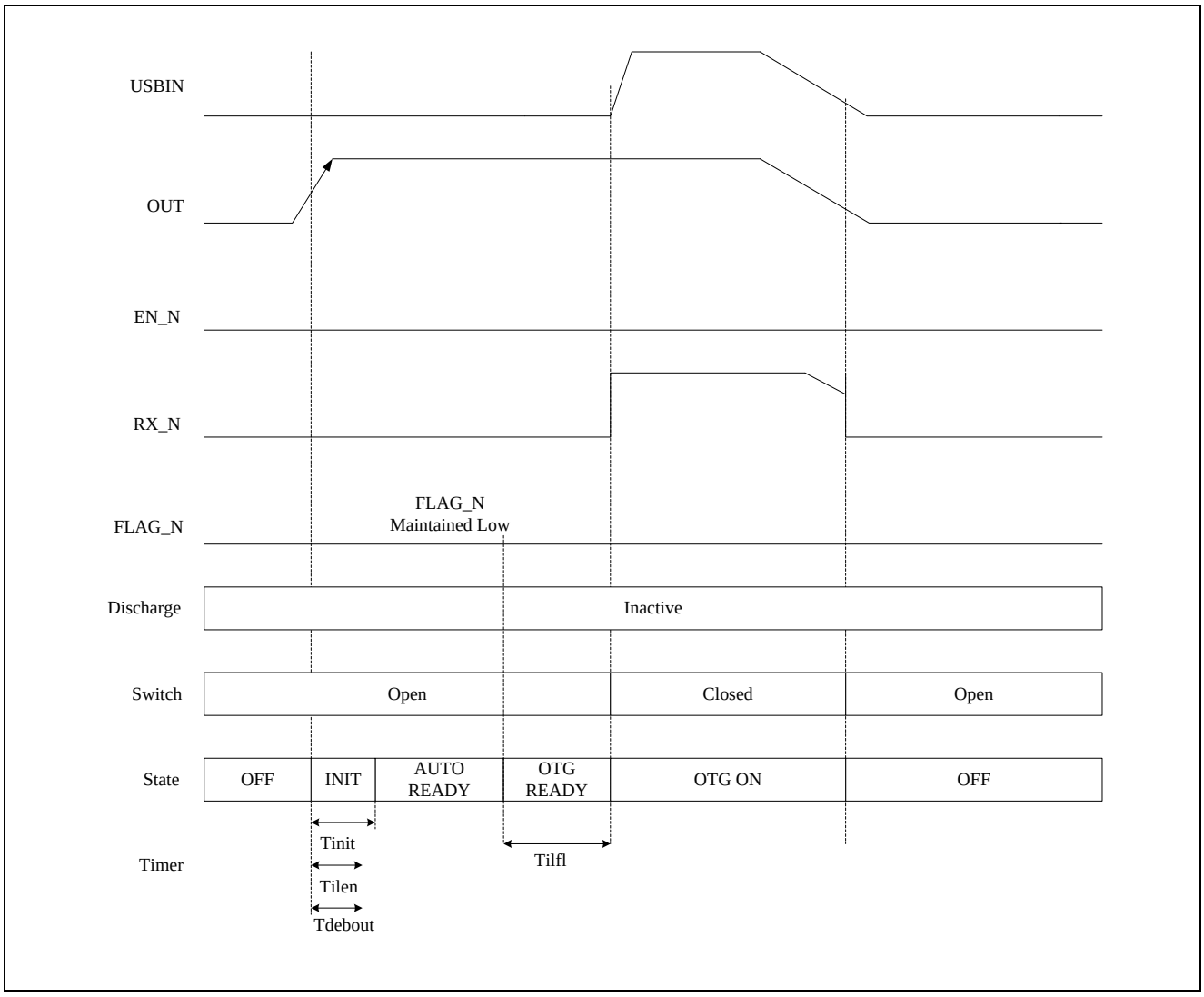


Figure 4. Autonomous configuration. Application of VOUT

Timing Diagrams(Continued)

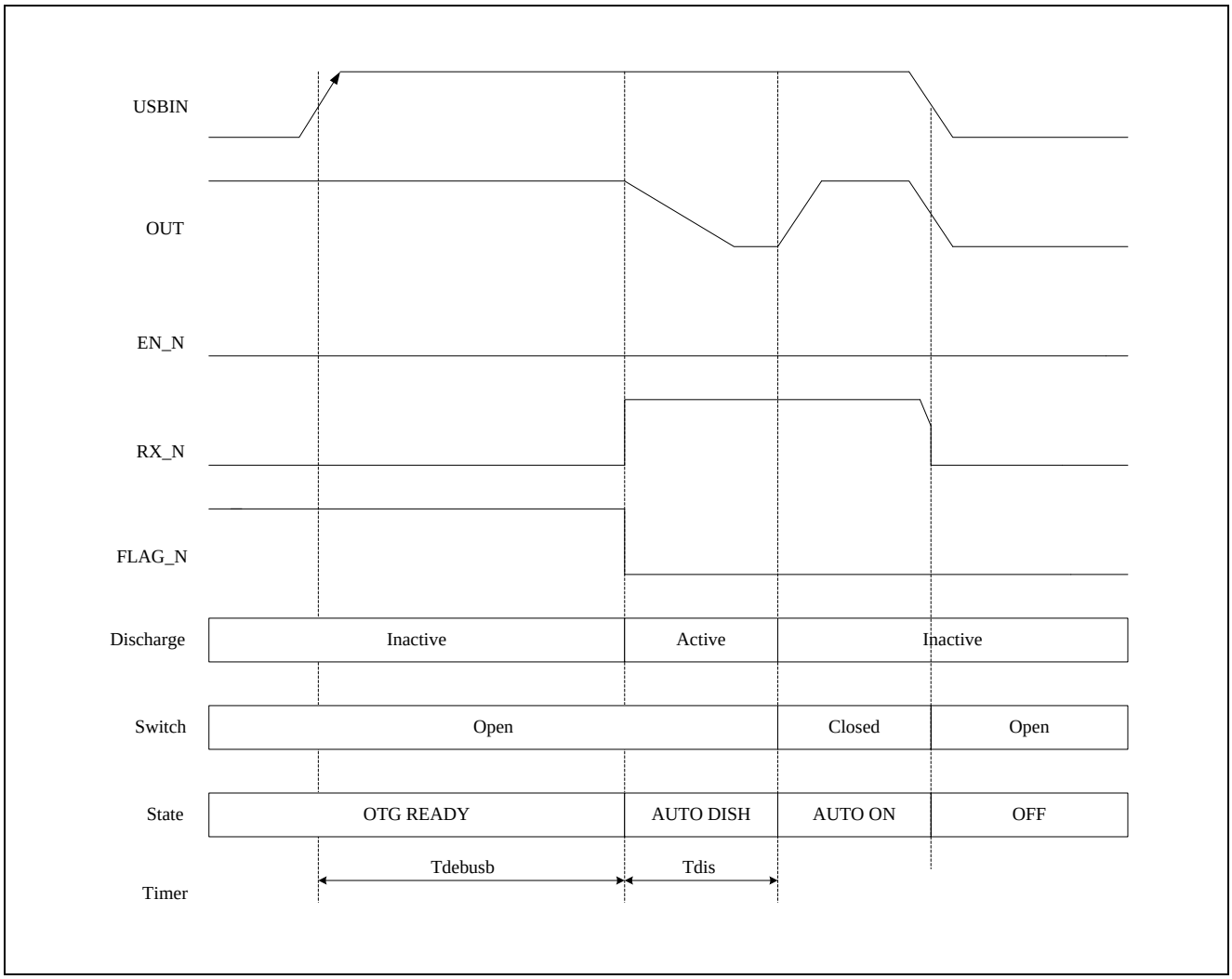


Figure 5. Autonomous configuration. Application of VBUS with VOUT present, removal of VBUS

Timing Diagrams(Continued)

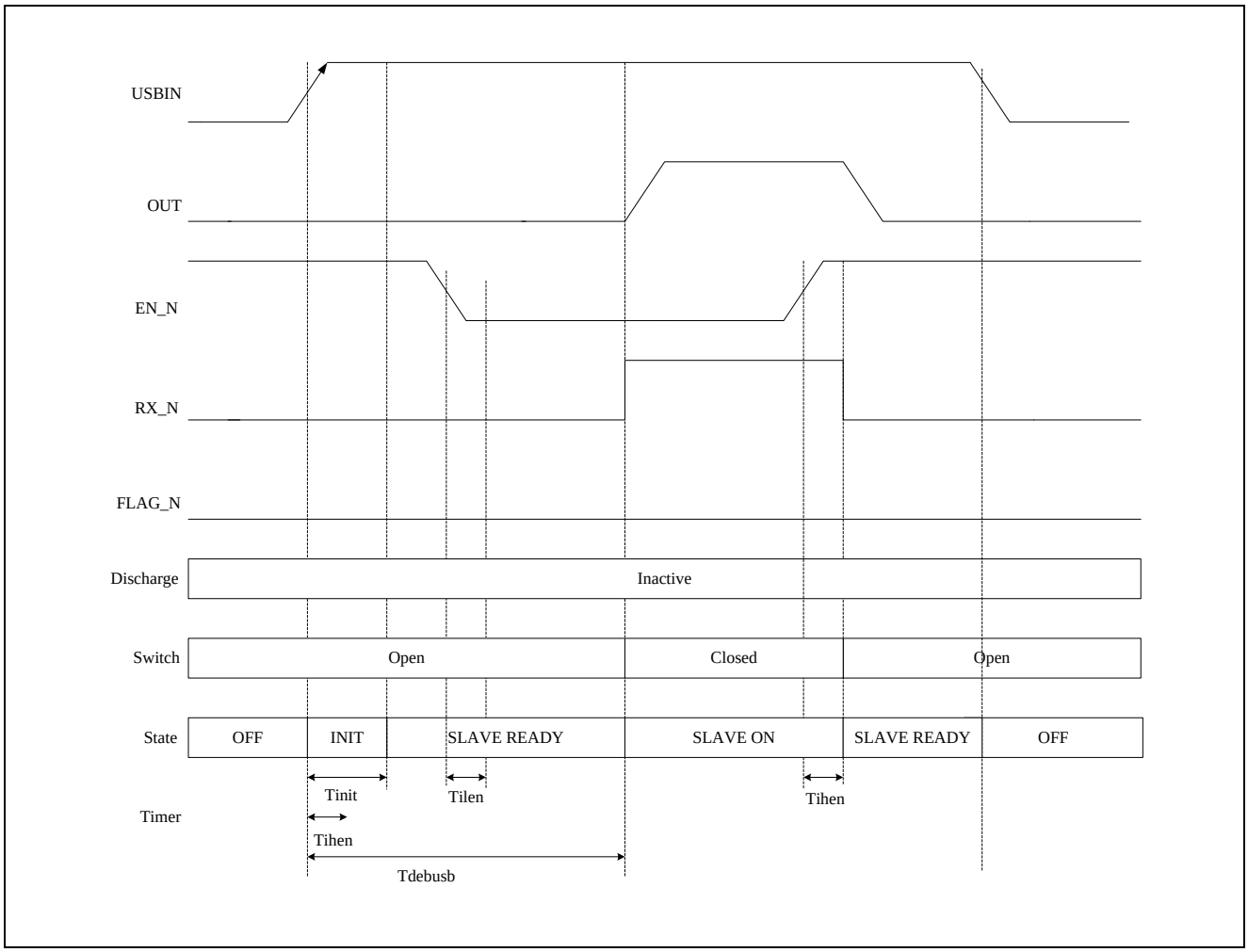


Figure 6. Slave configuration. Application of VBUS with system turned off, enabling, disabling

Timing Diagrams(Continued)

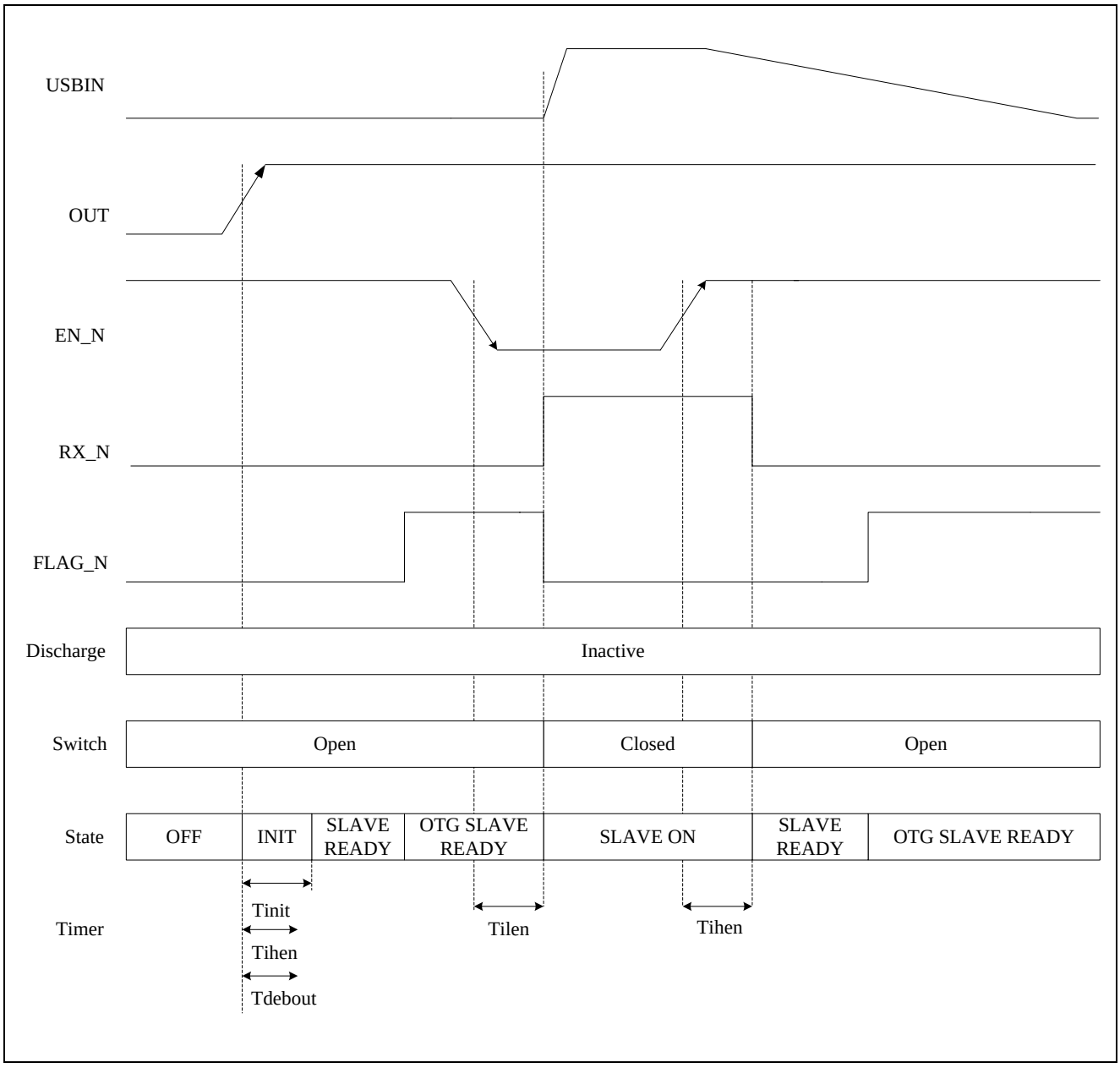
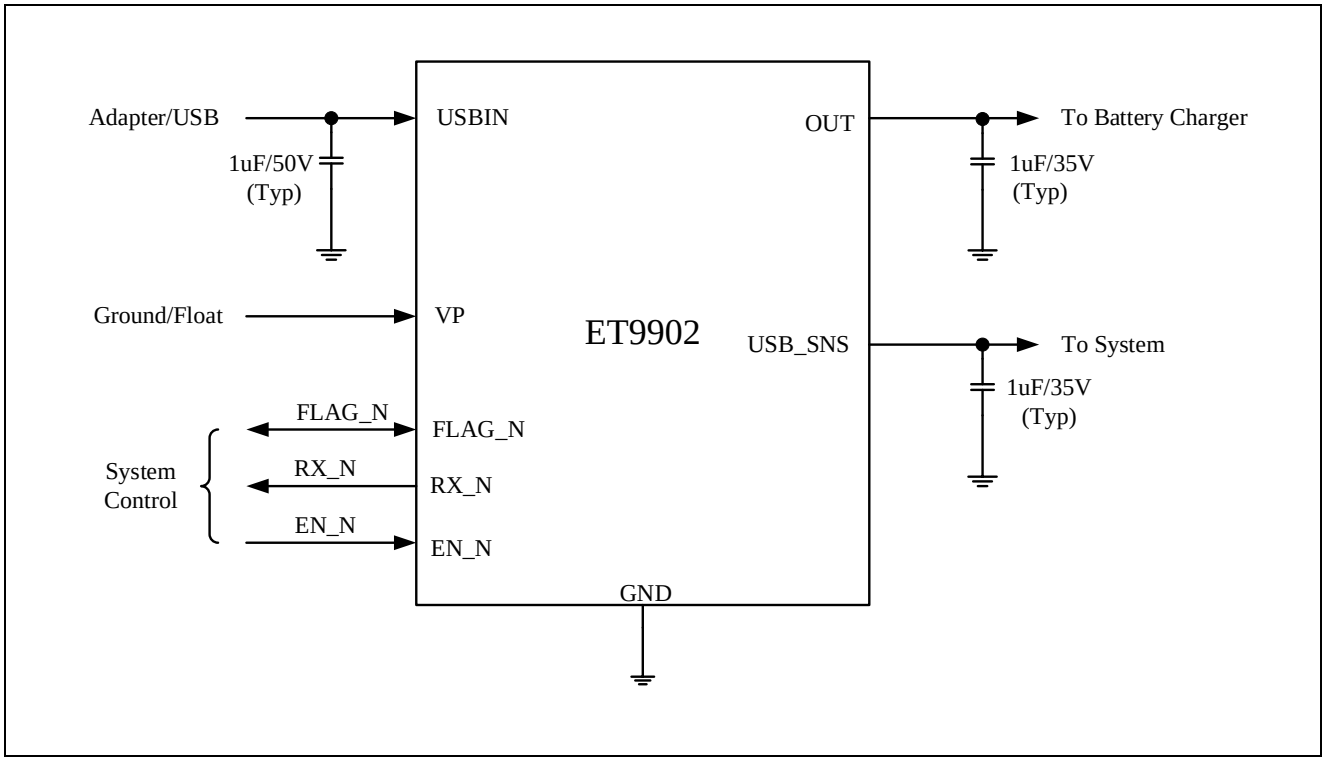


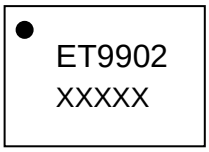
Figure 7. Slave configuration. Application of VOUT, enabling(OTG), disabling

Application Circuits



*: This application circuit is only for reference.

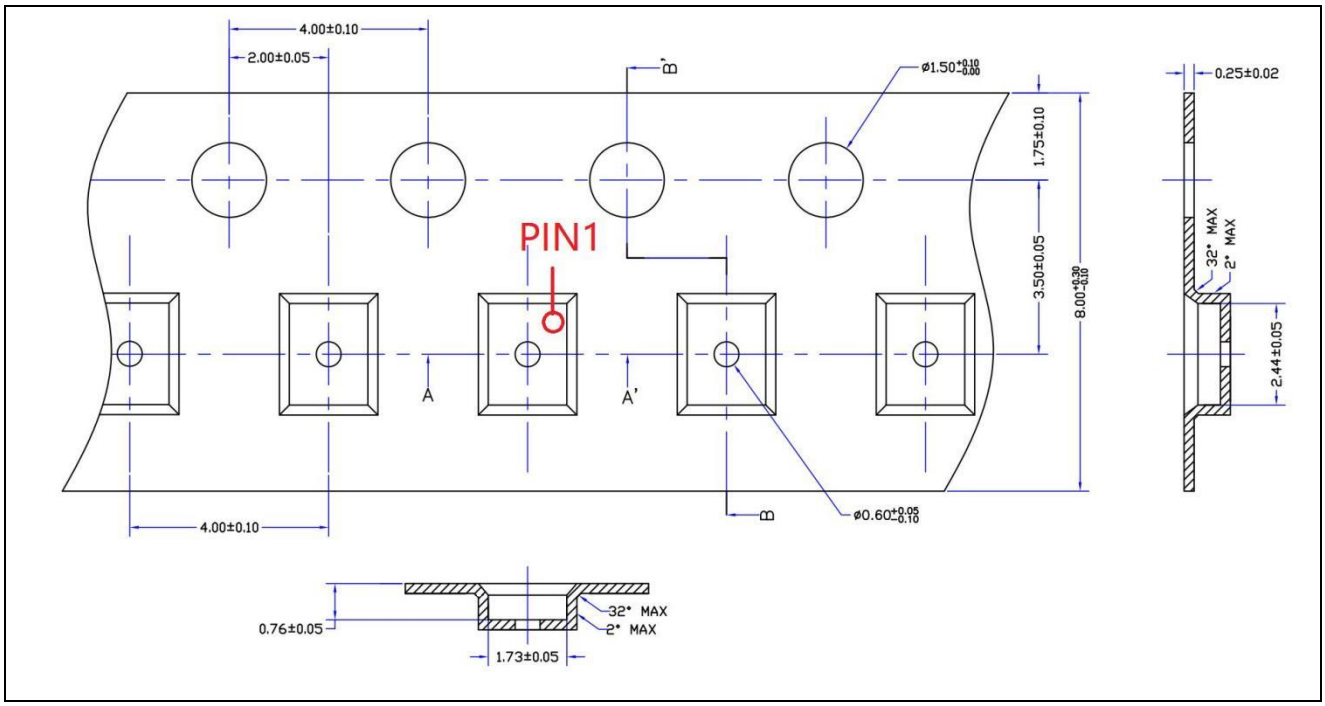
Marking



ET9902 - Part Number

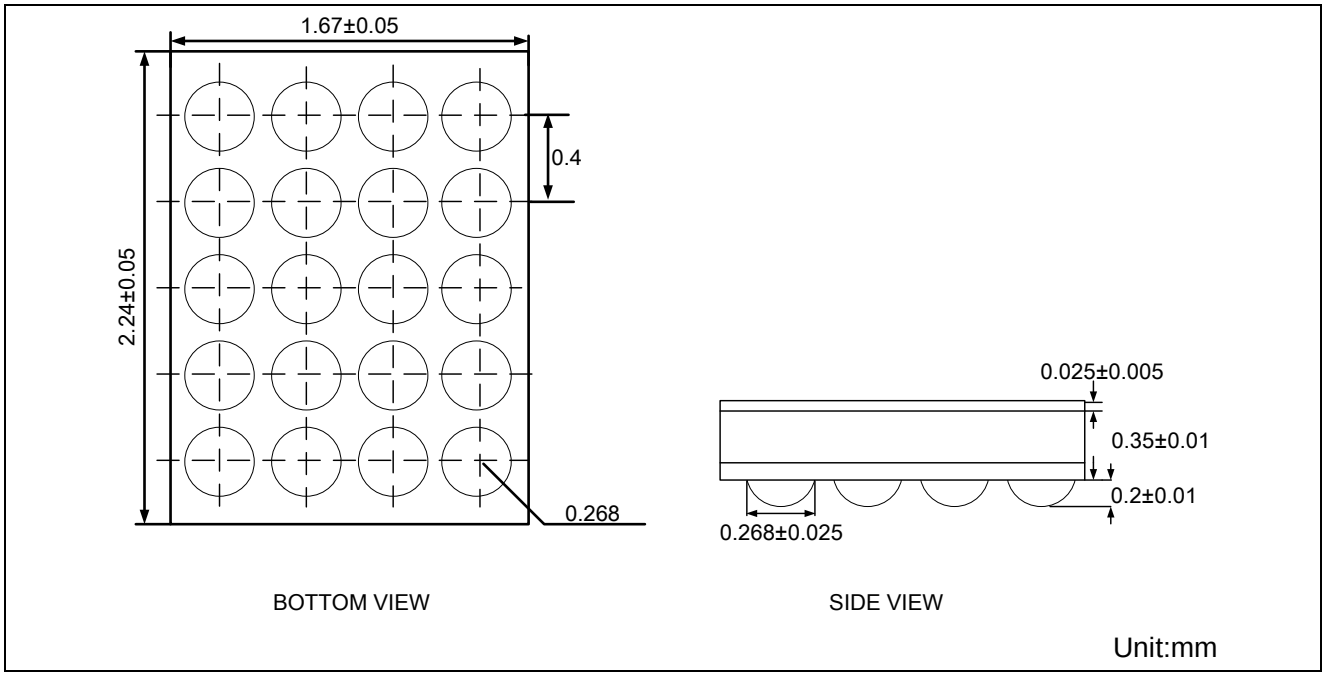
XXXXX - Tracking Number

Tape Information



Package Dimension

WLCSP20



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-6-3	Original Version	wum	wum	Liujy
1.1	2019-7-30	Add Marking &Tape Information	wum	wum	Liujy
1.2	2020-04-26	Document check and formalize	Shib	Shib	Liujy
1.3	2022-06-11	Update application circuit	Shib	Shib	Liujy
1.4	2022-07-08	Update EC table	Shib	Shib	Liujy
1.5	2022-07-19	Typo checking and add I_{SW2}	Shib	Shib	Liujy
1.6	2022-08-16	Update timing diagrams and application circuit	Shib	Shib	Liujy
1.7	2023-01-03	Add TVS characteristic	Wangp	Wangp	Liujy